CLAIMS

- 1. (Currently amended) An interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:
- (a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the low-frequency impedance of the tip/ring lines;
 - (b) high-frequency interface circuitry configured to process the high-frequency signals; and
- (c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:
- (1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines;
- (2) a coder/decoder (CODEC) configured to encode and decode the low-frequency signals; and
- (3) an impedance warping circuit (IWC) configured between the SLIC and the CODEC, wherein:

the IWC has first, second, and third differential ports, each port different from the other ports;

the IWC is configured to receive a first differential signal from the SLIC at the first differential port and a second differential signal from the CODEC at the second differential port and generate a third differential signal provided to the SLIC at the third differential port; and

the IWC tends to compensate for the effect of the blocking capacitor on the low-frequency impedance between the tip/ring lines.

- 2. (Original) The invention of claim 1, wherein the compensation provided by the IWC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.
- 3. (Original) The invention of claim 2, wherein the desired impedance has a resistance of about 900 ohms and a capacitance of about 2.16 microfarads.
- 4. (Original) The invention of claim 1, wherein: the high-frequency signals correspond to DSL signals having frequencies greater than about 4 kHz:

the low-frequency signals correspond to POTS signals having frequencies less than about 4 kHz; and

the filter circuitry comprises (i) a high-pass filter configured to provide the DSL signals to the high-frequency interface circuitry and (ii) a low-pass filter configured to provide the POTS signals to the low-frequency interface circuitry, wherein the blocking capacitor is part of the high-pass filter.

- 5. (Previously presented) The invention of claim 1, wherein the IWC is configured to receive a first differential signal from the SLIC and a second differential signal from the CODEC and generate a third differential signal provided to the SLIC.
 - 6. (Previously presented) The invention of claim 5, wherein the IWC comprises:
- (A) a first amplifier configured to generate a first single-ended output signal based on the second differential output signal; and
- (B) a second amplifier configured to generate a second single-ended output signal based on the first differential output signal, wherein the first and second single-ended output signals are used to generate the third differential output signal.

- 7. (Previously presented) The invention of claim 6, wherein:
 the first amplifier comprises a first operational amplifier configured as an inverter; and
 the second amplifier comprises a second operational amplifier configured as a frequencydependent inverter, such that the third differential output signal increases when frequency of the lowfrequency signals increases.
- 8. (Previously presented) The invention of claim 7, wherein the second amplifier further comprises a resistor and a compensating capacitor configured in parallel between the inverting input and the output of the second operational amplifier.
- 9. (Previously presented) The invention of claim 6, wherein the IWC further comprises an output filter configured to filter the first single-ended output signal generated by the first amplifier.
- 10. (Currently amended) An impedance warping circuit (IWC) for an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:
- (a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the low-frequency impedance of the tip/ring lines;
 - (b) high-frequency interface circuitry configured to process the high-frequency signals; and
- (c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:
- (1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines;
- (2) a coder/decoder (CODEC) configured to encode and decode the low-frequency signals; and
- (3) the IWC configured between the SLIC and the CODEC, wherein:

 the IWC has first, second, and third differential ports, each port different from the other ports;

the IWC is configured to receive a first differential signal from the SLIC at the first differential port and a second differential signal from the CODEC at the second differential port and generate a third differential signal provided to the SLIC at the third differential port; and

the IWC tends to compensate for the effect of the blocking capacitor on the low-frequency impedance between the tip/ring lines.

- 11. (Original) The invention of claim 10, wherein the compensation provided by the IWC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.
- 12. (Original) The invention of claim 11, wherein the desired impedance has a resistance of about 900 ohms and about 2.16 microfarads.
- 13. (Original) The invention of claim 10, wherein: the high-frequency signals correspond to DSL signals having frequencies greater than about 4 kHz;

the low-frequency signals correspond to POTS signals having frequencies less than about 4 kHz; and

the filter circuitry comprises (i) a high-pass filter configured to provide the DSL signals to the high-frequency interface circuitry and (ii) a low-pass filter configured to provide the POTS signals to the low-frequency interface circuitry, wherein the blocking capacitor is part of the high-pass filter.

- 14. (Previously presented) The invention of claim 10, wherein the IWC is configured to receive a first differential signal from the SLIC and a second differential signal from the CODEC and generate a third differential signal provided to the SLIC.
 - 15. (Previously presented) The invention of claim 14, wherein the IWC comprises:
- (A) a first amplifier configured to generate a first single-ended output signal based on the second differential output signal; and
- (B) a second amplifier configured to generate a second single-ended output signal based on the first differential output signal, wherein the first and second single-ended output signals are used to generate the third differential output signal.
- 16. (Previously presented) The invention of claim 15, wherein: the first amplifier comprises a first operational amplifier configured as an inverter; and the second amplifier comprises a second operational amplifier configured as a frequency-dependent inverter, such that the third differential output signal increases when frequency of the low-frequency signals increases.
- 17. (Previously presented) The invention of claim 16, wherein the second amplifier further comprises a resistor and a compensating capacitor configured in parallel between the inverting input and the output of the second operational amplifier.
- 18. (Previously presented) The invention of claim 15, wherein the IWC further comprises an output filter configured to filter the first single-ended output signal generated by the first amplifier.
- 19. (Previously presented) The invention of claim 1, wherein: the SLIC and the CODEC are adapted to synthesize a desired impedance between the tip and ring lines;

the blocking capacitor impedes the impedance synthesis by causing an effective impedance between the tip and ring lines to deviate from the desired impedance; and the IWC is adapted to reduce the impedance deviation caused by the blocking capacitor.

20. (Previously presented) The invention of claim 10, wherein: the SLIC and the CODEC are adapted to synthesize a desired impedance between the tip and ring lines;

the blocking capacitor impedes the impedance synthesis by causing an effective impedance between the tip and ring lines to deviate from the desired impedance; and the IWC is adapted to reduce the impedance deviation caused by the blocking capacitor.

21-22. (Canceled)

- 23. (Currently amended) An interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising filter circuitry having a blocking capacitor, the filter circuitry adapted to separate low-frequency and high-frequency signals appearing on the tip/ring lines between low-frequency and high-frequency signal paths, the low-frequency path including:
 - (1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines;
- (2) a coder/decoder (CODEC) configured to encode and decode the low-frequency signals; and
- (3) an impedance warping circuit (IWC) coupled between the SLIC and the CODEC, wherein:

the SLIC and the CODEC are adapted to synthesize a desired impedance between the tip and ring lines;

the blocking capacitor impedes the impedance synthesis by causing an effective impedance between the tip and ring lines to deviate from the desired impedance;

the IWC has first, second, and third differential ports, each port different from the other ports;

the IWC is configured to receive a first differential signal from the SLIC at the first differential port and a second differential signal from the CODEC at the second differential port and generate a third differential signal provided to the SLIC at the third differential port; and the IWC is adapted to reduce the impedance deviation caused by the blocking capacitor.

24. (Canceled)

- 25. (Currently amended) An impedance warping circuit (IWC) for an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising filter circuitry having a blocking capacitor, the filter circuitry adapted to separate low-frequency and high-frequency signals appearing on the tip/ring lines between low-frequency and high-frequency signal paths, the low-frequency path including:
 - (1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines;
- (2) a coder/decoder (CODEC) configured to encode and decode the low-frequency signals; and
- (3) an impedance warping circuit (IWC) coupled between the SLIC and the CODEC, wherein:

the SLIC and the CODEC are adapted to synthesize a desired impedance between the tip and ring lines;

the blocking capacitor impedes the impedance synthesis by causing an effective impedance between the tip and ring lines to deviate from the desired impedance;

the IWC has first, second, and third differential ports, each port different from the other ports;

the IWC is configured to receive a first differential signal from the SLIC at the first differential port and a second differential signal from the CODEC at the second differential port and generate a third differential signal provided to the SLIC at the third differential port; and the IWC is adapted to reduce the impedance deviation caused by the blocking capacitor.

26. (Canceled)